19-0554; Rev 0; 5/06

EVALUATION KIT AVAILABLE

Complete VGA 1:2 or 2:1 Multiplexer

General Description

The MAX4885 integrates high-bandwidth analog switches and level-translating buffers to implement a complete 1:2 or 2:1 multiplexer for VGA signals. The device provides switching for RGB, display data channel (DDC), and horizontal and vertical synchronization (HSYNC, VSYNC) signals. A low-noise charge pump with internal capacitors provides a boosted gate-drive voltage to improve performance of the RGB switches.

In the 1:2 multiplexer mode, HSYNC/VSYNC inputs feature level-shifting buffers to support low-voltage CMOS or standard TTL-compatible graphics controllers. In the 2:1 multiplexer mode, the output buffers for the HSYNC/VSYNC inputs are disabled, allowing bidirectional signaling. In both modes, DDC signals are voltage-clamped to an external voltage to provide level translation and protection. The MAX4885 features a 5µA shutdown mode and is ESD protected to ±8kV Human Body Model (HBM) on externally routed pins.

The MAX4885 is specified over the extended (-40°C to +85°C) temperature range, and is available in the 32-pin, 5mm x 5mm TQFN package.

Applications

Notebook Computers

Digital Projectors

Computer Monitors

Servers

KVM Switches

Features

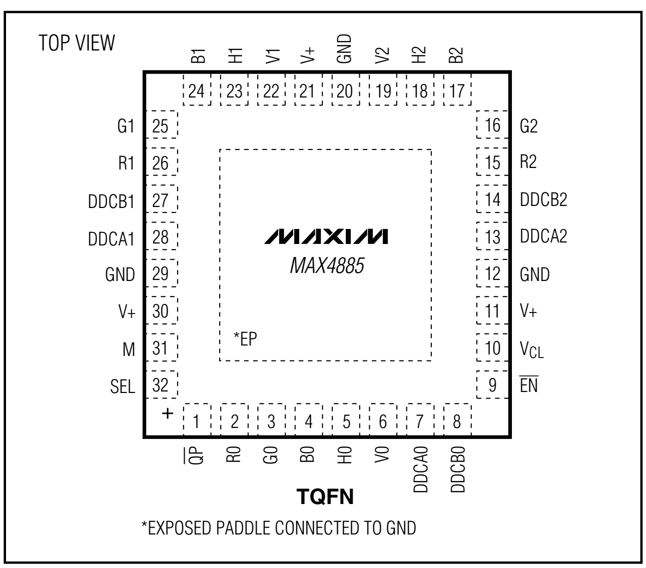
- ♦ +5V Single-Supply Operation
- ♦ Programmable Voltage Clamp for Open-Drain DDC Signals
- ♦ Low 5Ω (typ) On-Resistance (R, G, B Signals)
- ♦ Low 13pF (typ) On-Capacitance (R, G, B Signals)
- ♦ Break-Before-Make Switching Protects Against Circuit Shorts
- ♦ ±8kV HBM ESD Protection on Externally Routed Pins
- ♦ Low 300µA Supply Current (Lower than 1µA with Charge Pump Disabled)
- ♦ Space-Saving, Lead-Free, 32-Pin (5mm x 5mm) TQFN Package

Ordering Information

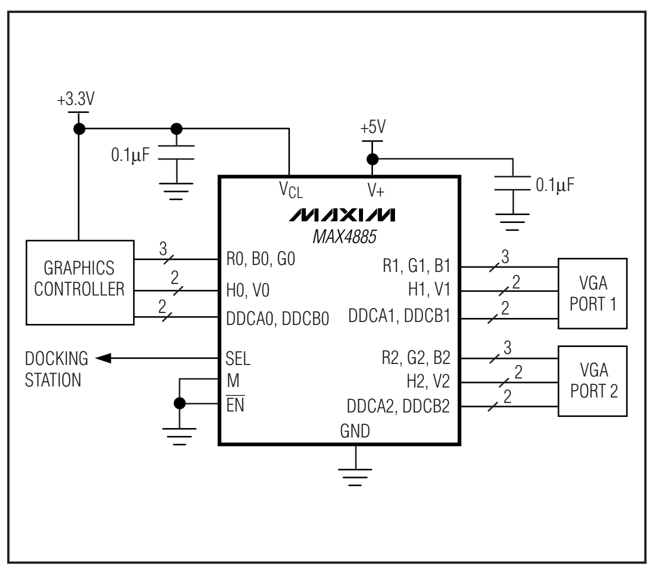
PART	TEMP RANGE	PIN-PACKAGE	PKG CODE
MAX4885ETJ+	-40°C to +85°C	32 TQFN-EP*	T3255-4

*EP = Exposed pad.
+Denotes lead-free package.

Pin Configuration



Typical Operating Circuit



ABSOLUTE MAXIMUM RATINGS

(All voltages referenced to GND.)
V_+, V_{CL} ....-0.3V to +6V
R_, G_, B_, DDCA_, DDCB_, SEL, M,
$\overline{EN}$, $\overline{QP}$ (Note 1) ....-0.3V to V+ + 0.3V
H_, V_ ....-0.3V to +6V
Continuous Current Through RGB Switches ....±70mA
Continuous Current Through HV, DDC Switches…..........±50mA
Peak Current Through RGB Switches
(pulsed at 1ms, 10% duty cycle)................................±140mA
Peak Current Through HV, DDC Switches (pulsed at 1ms,
10% duty cycle)..±100mA

Continuous Power Dissipation (T_A = +70°C)
32-Pin TQFN (derate 21.3mW/°C above +70°C) 1702mW
Operating Temperature Range ....-40°C to +85°C
Storage Temperature Range ....-65°C to +150°C
Junction Temperature...+150°C
Lead Temperature (soldering, 10s) ....+300°C

Note 1: Signals exceeding V+ or GND are clamped by internal diodes. Limit forward-diode current to maximum current rating.

Stresses beyond those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

ELECTRICAL CHARACTERISTICS

(V+ = +5.0V ±10%, V_{CL} = +3.3V ±10%, T_A = T_{MIN} to T_{MAX}, $\overline{QP}$ = GND, unless otherwise noted. Typical values are at V+ = +5.0V, V_{CL} = +3.3V and T_A = +25°C.)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Supply Voltage Range	V+			4.5		5.5	V
Clamp Voltage Range	V_{CL}			2.7		V+	V
V_+ Quiescent Supply Current	I_+	V+ = +5.5V	$\overline{QP}$ = GND		0.3	0.5	mA
			$\overline{QP}$ = V+			1	µA
V_{CL} Quiescent Supply Current	I_{CL}	V_{CL} = V+ = +5.5V				1	µA
V_+ Shutdown Current	I_{+SHDN}	V+ = +5.5V, all digital inputs to V+ or GND				5	µA
V_{CL} Shutdown Current	I_{CLSHDN}	V_{CL} = V+ = +5.5V, all digital inputs to V+ or GND				1	µA
RGB ANALOG SWITCHES							
On-Resistance	R_{ON}	0V < V_{IN} < +2.5V, I_{IN} = -40mA	$\overline{QP}$ = GND		5	7.5	Ω
			$\overline{QP}$ = V+		6	10	
On-Resistance Matching	ΔR_{ON}	0V < V_{IN} < +2.5V, I_{IN} = -40mA			0.5	1.5	Ω
On-Resistance Flatness	$R_{FLAT(ON)}$	0V < V_{IN} < +2.5V, I_{IN} = -40mA			0.02	0.75	Ω
Off-Leakage Current	$I_{L(OFF)}$	R_, G_, B_ = 0V or +5.5V, $\overline{EN}$ = GND		-1		+1	µA
On-Leakage Current	$I_{L(ON)}$	R_, G_, B_ = 0V or +5.5V, $\overline{EN}$ = V+		-1		+1	µA
Charge Injection	Q	R_, G_, B_ = 0V, C_L = 1000pF	$\overline{QP}$ = GND		10		pC
			$\overline{QP}$ = V+		8		
HV MULTIPLEXER							
Input-Voltage Low	V_{ILHV}	M = GND				0.8	V
Input-Voltage High	V_{IHHV}	M = GND		2.0			V
High-Output Drive Current	I_{OHHV}	V_{OUT} = V_+ - 0.5V, M = GND		-16			mA
Low-Output Drive Current	I_{OLHV}	V_{OUT} = +0.5V, M = GND				+16	mA
On-Resistance	R_{ONHV}	H_ = V_ = +2.5V, I_{IN} = -40mA, M = V+				15	Ω
Charge Injection	Q	H_, V_ = 0V, M = V+, C_L = 1000pF			21		pC

ELECTRICAL CHARACTERISTICS (continued)

($V+ = +5.0V \pm 10\%$, $V_{CL} = +3.3V \pm 10\%$, $T_A = T_{MIN}$ to T_{MAX}, $\overline{QP}$ = GND, unless otherwise noted. Typical values are at $V+ = +5.0V$, $V_{CL} = +3.3V$ and $T_A = +25°C$.)

PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
DDC MULTIPLEXER						
On-Resistance	$R_{ON(DDC)}$	$V_{IN} < +0.4V$, $V_{CL} = +3.0V$, $I_{IN} = -20mA$			20	Ω
DDC Leakage	$I_{L(DDC)}$	$V_{CL} - 0.4V < V_{OUT} < V_{CL}$, $V_{IN} = V+$	-1		+1	µA
Charge Injection	Q	DDCA_, DDCB_ = 0V, C_L = 1000pF		10		pC
SWITCH LOGIC (SEL, M, $\overline{EN}$, $\overline{QP}$)						
Input-Low Voltage	V_{IL}	V+ = +5.5V			0.8	V
Input-High Voltage	V_{IH}	V+ = +4.5V	2.0			V
Input Leakage Current	I_{LEAK}	V_{IN} = V+	-1		+1	µA
ESD PROTECTION						
ESD Protection		Human Body Model, all pins		±2		kV
		Human Body Model, R_, G_, B_, H_, V_, DDCA_, DDCB_		±8		kV

AC ELECTRICAL CHARACTERISTICS

($V+ = +5.0V \pm 10\%$, $V_{CL} = +3.3V \pm 10\%$, $T_A = T_{MIN}$ to T_{MAX}, $\overline{QP}$ = GND. Typical values are at $V+ = +5.0V$, $V_{CL} = +3.3V$ and $T_A = +25°C$, unless otherwise noted.) (Note 2)

PARAMETER	SYMBOL	CONDITIONS		MIN	TYP	MAX	UNITS
Bandwidth	f_{MAX}	$R_S = R_L = 50\Omega$	$\overline{QP}$ = GND		350		MHz
			$\overline{QP}$ = V+		350		
Insertion Loss	I_{LOS}	1MHz < f < 50MHz, $R_S = R_L = 50\Omega$	$\overline{QP}$ = GND		0.85	1.2	dB
			$\overline{QP}$ = V+		1	1.6	
Crosstalk	V_{CT}	1MHz < f < 50MHz, $V_{IN} = 0.7V_{P-P}$, $R_S = R_L = 50\Omega$			-40		dB
Off-Capacitance	C_{OFF}	f = 1MHz, $\overline{QP}$ = GND or V+			5		pF
On-Capacitance	C_{ON}	f = 1 MHz	$\overline{QP}$ = GND		13		pF
			$\overline{QP}$ = V+		17		
Charge-Pump Noise	V_{NQP}	$V_{IN} = +1.0V$, $R_S = R_L = 50\Omega$			50	200	µV

TIMING CHARACTERISTICS

(V+ = +5.0V ±10%, V_{CL} = +3.3V ±10%, T_A = T_{MIN} to T_{MAX}, $\overline{QP}$ = GND. Typical values are at V+ = +5.0V, V_{CL} = +3.3V and T_A = +25°C, unless otherwise noted.) (Note 2)

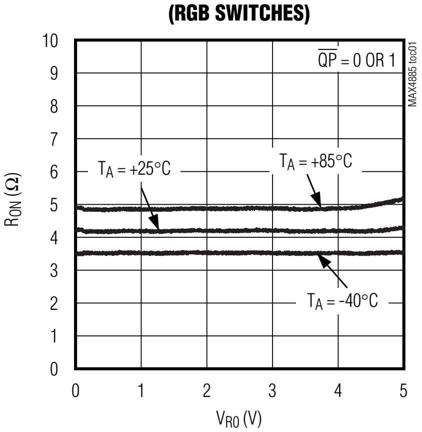
PARAMETER	SYMBOL	CONDITIONS	MIN	TYP	MAX	UNITS
Charge-Pump Startup Time	t_{QPON}			150		µs
RGB ANALOG SWITCHES						
Turn-On Time	t_{ON}	V_{IN} = +1.0V, R_L = 100Ω, Figure 1			7	µs
Turn-Off Time	t_{OFF}	V_{IN} = +1.0V, R_L = 100Ω, Figure 1		0.1		µs
Propagation Delay	t_{PD}	C_L = 10pF, Figure 2, R_L = R_S = 50Ω		0.1		ns
Output Skew Between Ports	t_{SKEW}	C_L = 10pF, Skew between any two ports: R, G, B. Figure 2, R_S = R_L = 50Ω		30		ps
HV MULTIPLEXER						
Turn-On Time	t_{ON}	M = 0, Figure 1			5	µs
Turn-Off Time	t_{OFF}	M = 0, Figure 1		0.1		µs
Propagation Delay	t_{PD}	C_L = 10pF, M = GND		6	16	ns
		C_L = 10pF, M = V+		0.1		ns
DDC MULTIPLEXER						
Turn-On Time	t_{ON}	V_{IN} = +1.0V, R_L = 100Ω, Figure 1			5	µs
Turn-Off Time	t_{OFF}	V_{IN} = +1.0V, R_L = 100Ω, Figure 1		0.1		µs
Propagation Delay	t_{PD}	C_L = 10pF, Figure 2		0.25		ns

Note 2: Timing parameters are guaranteed by design and correlation over the full operating temperature range.

Typical Operating Characteristics

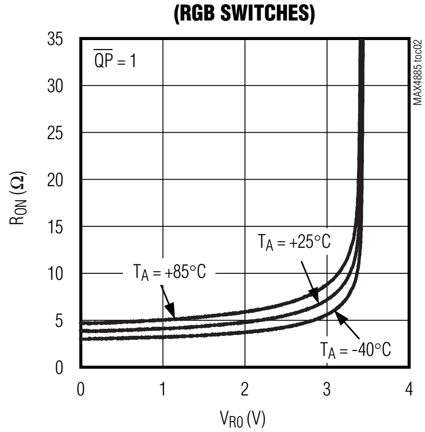
(V+ = +5.0V, V_{CL} = +3.3V and T_A = +25°C, unless otherwise noted.)

R_{ON} vs. V_{R0}* (RGB SWITCHES)



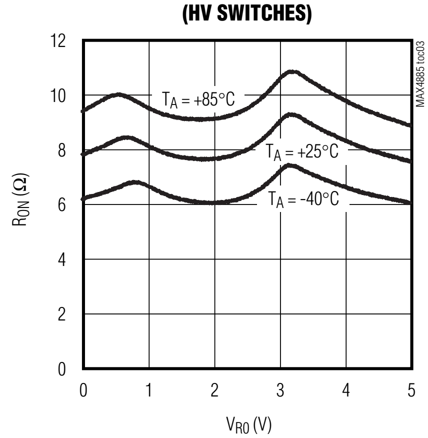
*R0, G0, B0 ARE INTERCHANGEABLE.

R_{ON} vs. V_{R0}* (RGB SWITCHES)



*R0, G0, B0 ARE INTERCHANGEABLE.

R_{ON} vs. V_{R0}* (HV SWITCHES)

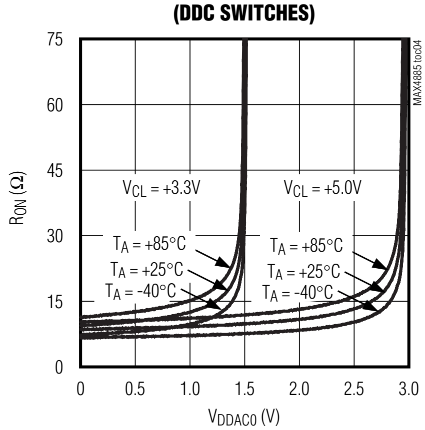


*R0, G0, B0 ARE INTERCHANGEABLE.

Typical Operating Characteristics (continued)

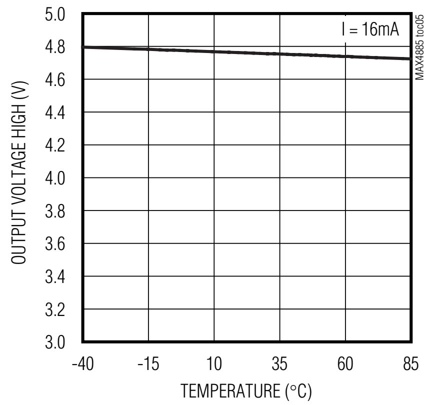
($V+ = +5.0V$, $V_{CL} = +3.3V$ and $T_A = +25°C$, unless otherwise noted.)

R_{ON} vs. V_{DDAC0}* (DDC SWITCHES)

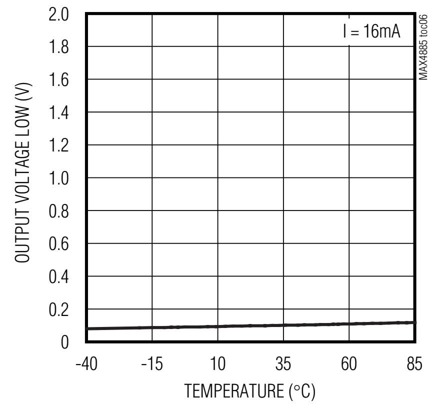


*DDAC0 AND DDCB0 ARE INTERCHANGEABLE.

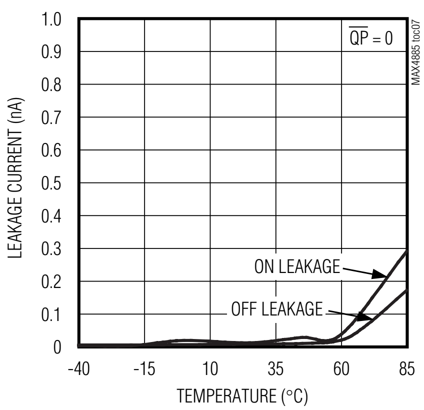
HV BUFFER OUTPUT VOLTAGE HIGH vs. TEMPERATURE



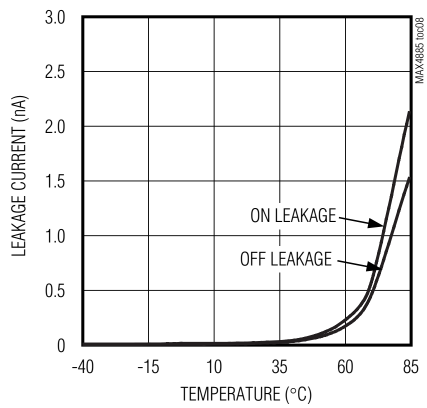
HV BUFFER OUTPUT VOLTAGE LOW vs. TEMPERATURE



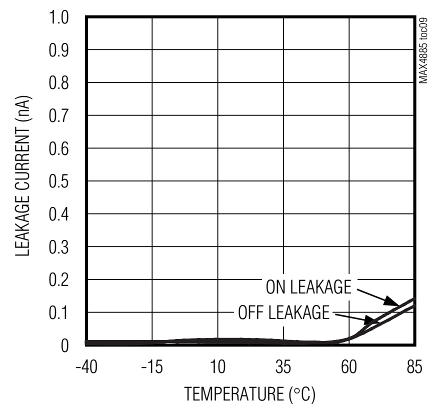
RGB LEAKAGE CURRENT vs. TEMPERATURE



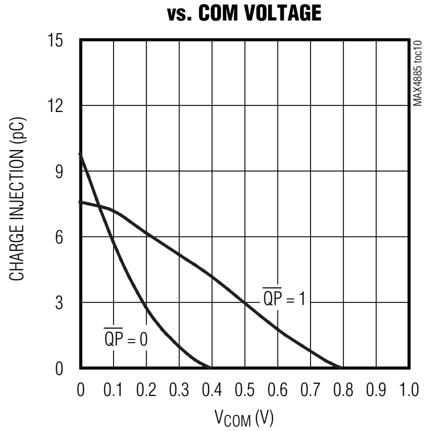
HV LEAKAGE CURRENT vs TEMPERATURE



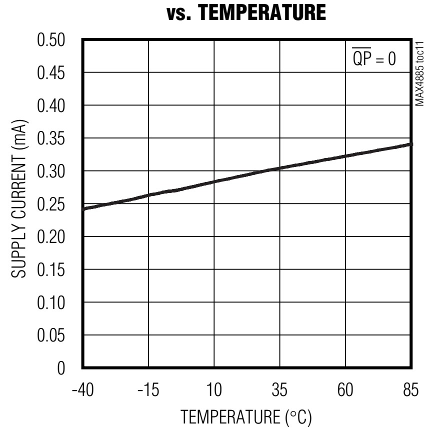
DDC LEAKAGE CURRENT vs. TEMPERATURE



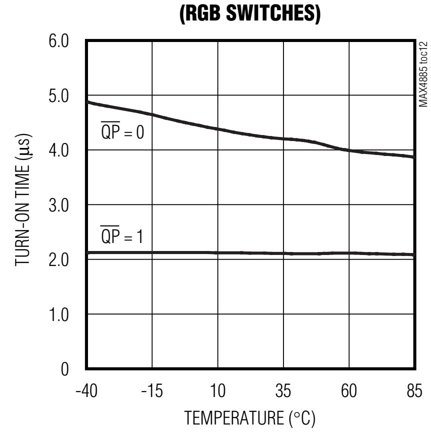
RGB CHARGE INJECTION vs. COM VOLTAGE



SUPPLY CURRENT vs. TEMPERATURE



t_{ON} vs. TEMPERATURE (RGB SWITCHES)

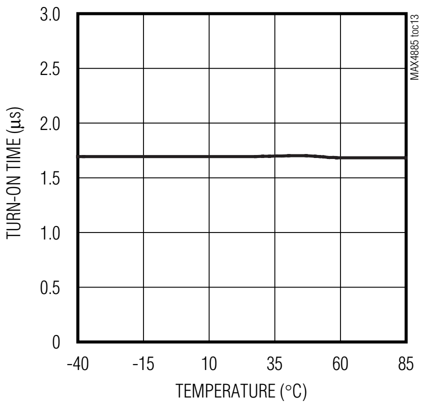


Complete VGA 1:2 or 2:1 Multiplexer

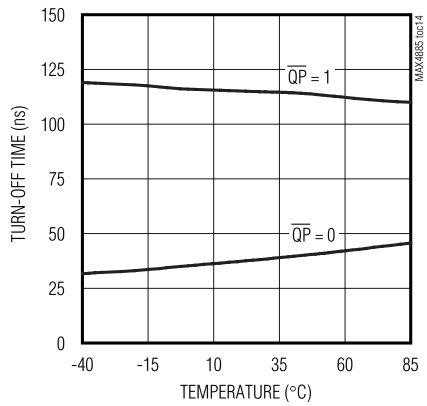
Typical Operating Characteristics (continued)

($V+ = +5.0V$, $V_{CL} = +3.3V$ and $T_A = +25°C$, unless otherwise noted.)

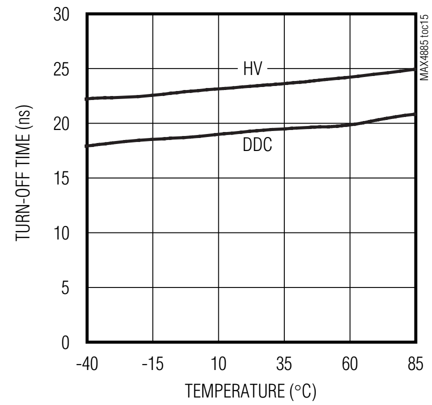
t_{ON} vs. TEMPERATURE (HV, DDC SWITCHES)



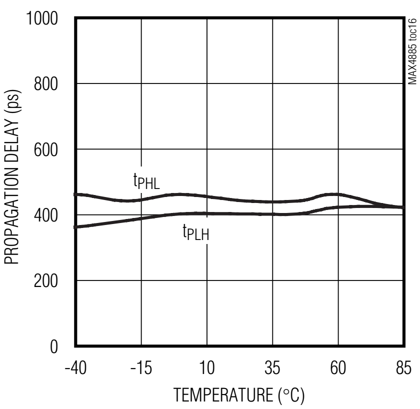
t_{OFF} vs. TEMPERATURE (RGB SWITCHES)



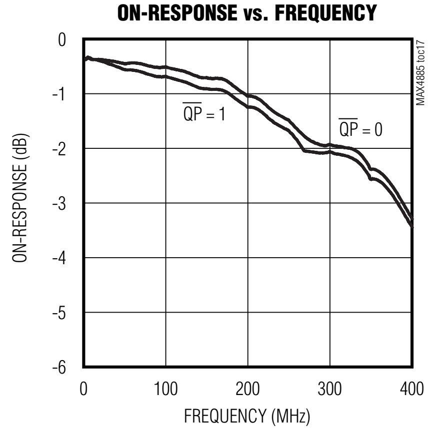
t_{OFF} vs. TEMPERATURE (HV, DDC SWITCHES)



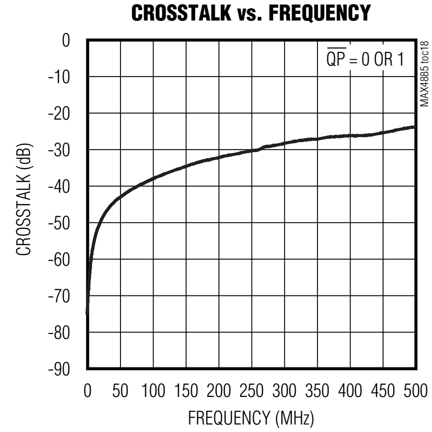
RGB PROPAGATION DELAY vs. TEMPERATURE



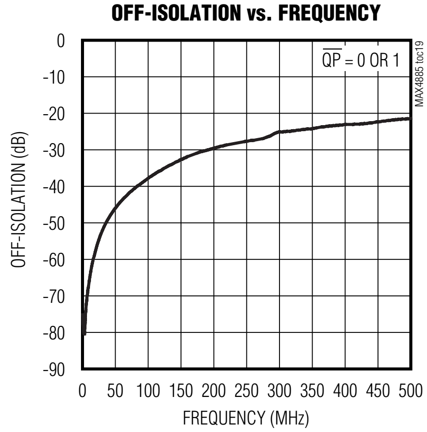
ON-RESPONSE vs. FREQUENCY



CROSSTALK vs. FREQUENCY



OFF-ISOLATION vs. FREQUENCY



Timing Circuits/Timing Diagrams

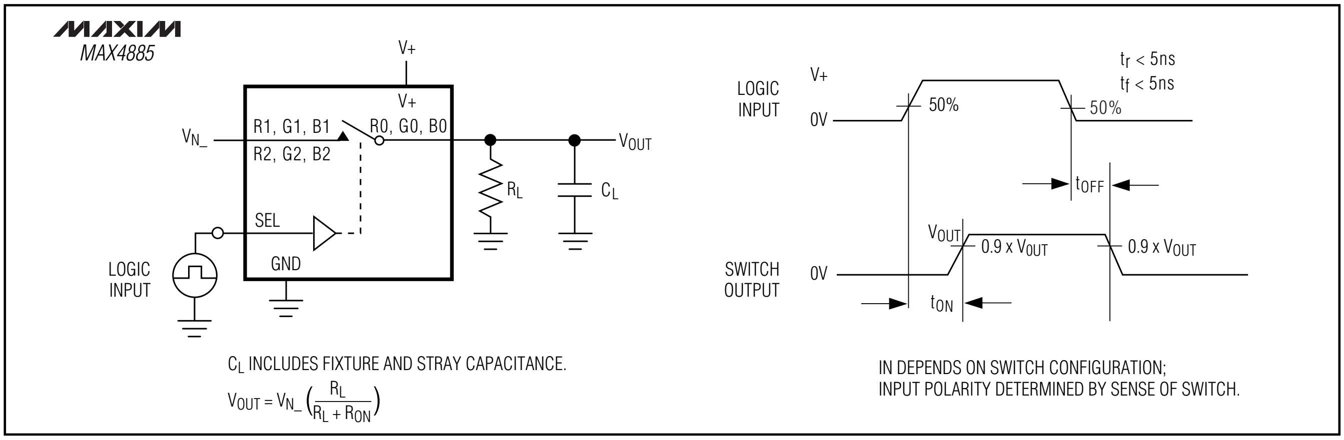


Figure 1. Switching Time

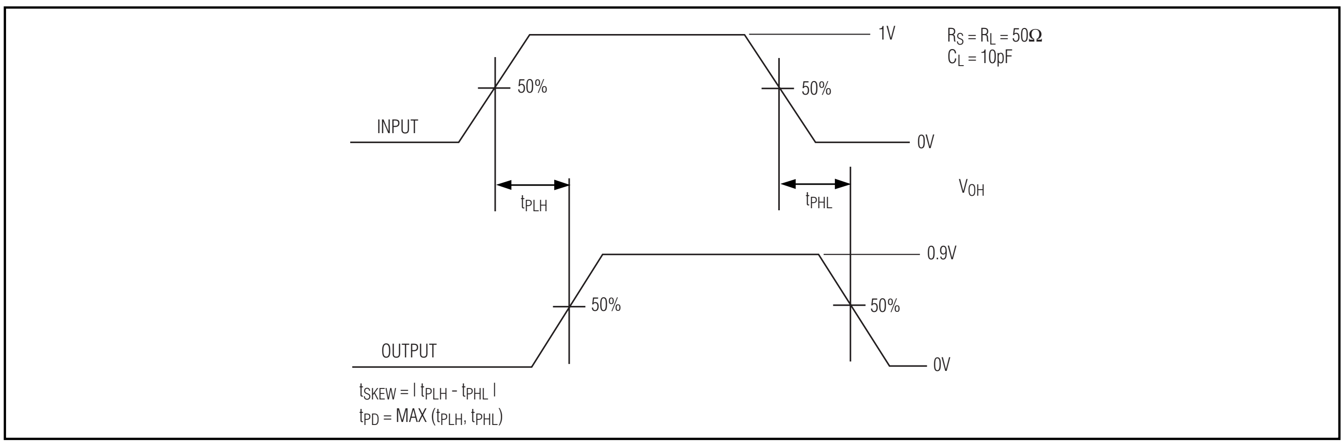


Figure 2. Propagation Delay and Skew Waveforms

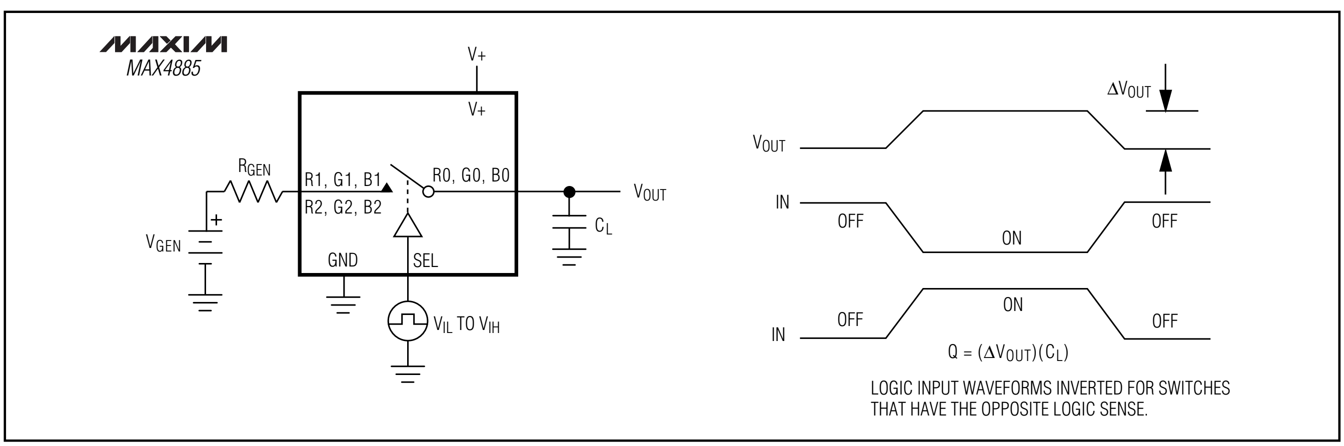


Figure 3. Charge Injection

Timing Circuits/Timing Diagrams (continued)

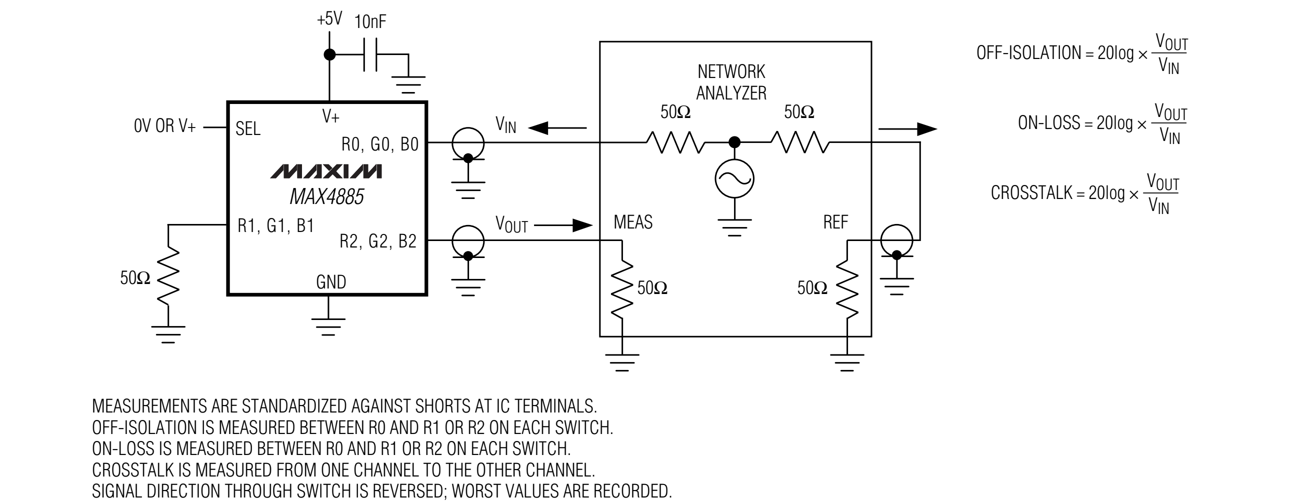


Figure 4. On-Loss, Off-Isolation, and Crosstalk

Pin Description

PIN	NAME	FUNCTION
1	$\overline{QP}$	Charge-Pump Enable, Active Low. Drive $\overline{QP}$ low for normal operation. Drive $\overline{QP}$ high to disable the internal charge pump.
2	R0	RGB Analog I/O
3	G0	RGB Analog I/O
4	B0	RGB Analog I/O
5	H0	Horizontal Sync I/O
6	V0	Vertical Sync I/O
7	DDCA0	DDC I/O
8	DDCB0	DDC I/O
9	$\overline{EN}$	Enable Input, Active Low. Drive $\overline{EN}$ low for normal operation. Drive $\overline{EN}$ high to disable the device. All I/Os are high-impedance and charge pump is off when the device is disabled.
10	V_{CL}	DDC Clamp Voltage. Open-drain DDCA_ and DDCB_ outputs are clamped to one diode-drop below V_{CL}. +2.7V < V_{CL} < V+. Connect V_{CL} to +3.3V for voltage clamping, or connect to V+ to disable clamping. Bypass V_{CL} to GND with a 0.1µF or larger ceramic capacitor.
11, 21, 30	V+	Supply Voltage. V+ = +5.0V ± 10%. Bypass each to GND with a 0.1µF or larger ceramic capacitor.
12, 20, 29	GND	Ground
13	DDCA2	DDC I/O
14	DDCB2	DDC I/O
15	R2	RGB Analog I/O
16	G2	RGB Analog I/O
17	B2	RGB Analog I/O

Pin Description (continued)

PIN	NAME	FUNCTION
18	H2	Horizontal Sync I/O
19	V2	Vertical Sync I/O
22	V1	Vertical Sync I/O
23	H1	Horizontal Sync I/O
24	B1	RGB Analog I/O
25	G1	RGB Analog I/O
26	R1	RGB Analog I/O
27	DDCB1	DDC I/O
28	DDCA1	DDC I/O
31	M	Mode Select. Drive M low for 1:2 multiplexer mode. Drive M high for 2:1 multiplexer mode. See Tables 1, 2, and 3.
32	SEL	Select. Logic input for switching RGB, HV, and DDC switches. See Tables 1, 2, and 3.
EP	EP	Exposed Pad. Connect exposed pad to ground.

Detailed Description

The MAX4885 integrates high-bandwidth analog switches and level-translating buffers to implement a complete 1:2 or 2:1 multiplexer for VGA signals. The device provides switching for RGB, HSYNC, VSYNC, and DDC signals. A low-noise charge pump with internal capacitors provides a boosted gate-drive voltage to improve performance of the RGB switches.

The device provides two modes of operation: 1:2 and 2:1. In 1:2 mode (M = 0), the HSYNC and VSYNC inputs feature level-shifting buffers to support TTL output logic levels from low-voltage graphics controllers. These buffered switches may be driven from as little as +2.0V up to +5.5V. In 2:1 mode (M=1), the output buffers for the HSYNC and VSYNC signals are disabled. In both modes, RGB signals are routed with the same high-performance analog switches, and DDC signals are voltage clamped to a diode drop less than V_{CL}. Voltage clamping provides protection and compatibility with DDC signals and low-voltage ASICs. In keyboard/video/mouse (KVM) applications, V_{CL} is normally set to +5V because low-voltage clamping is not required, as specified by the VESA standard.

Drive $\overline{EN}$ logic high to shut down the MAX4885. In shutdown mode, supply current is reduced to 5µA and all switches are high impedance, providing high-signal rejection. The RGB, HSYNC, VSYNC, and DDC switches are ESD protected to ±8kV by the Human Body Model.

Table 1. RGB Truth Table

$\overline{EN}$	SEL	FUNCTION
0	0	R0 to R1 G0 to G1 B0 to B1
0	1	R0 to R2 G0 to G2 B0 to B2
1	X	R_, B_, and G_, High Impedance

X = Don't Care

RGB Switches

The MAX4885 provides three SPDT high-bandwidth switches to route standard VGA R, G, and B signals (see Table 1). A boosted gate-drive voltage is generated by an internal charge pump to improve performance of the RGB switches. The R, G, and B analog switches are identical, and any of the three switches can be used to route red, green, or blue video signals. The RGB switches function with reduced performance with the charge pump disabled.

Charge Pump

A low-noise charge pump with internal capacitors provides a doubled voltage for driving the RGB analog switches. Noise voltage from the charge pump is less than $50\mu V_{P-P}$. The noise level is more than 80dB below the signal level, making the charge pump suitable for standard VGA signals. The charge pump can be disabled to eliminate charge-pump noise; however, RGB switch performance is slightly degraded. Connect $\overline{QP}$ to ground for normal operation.

Horizontal/Vertical Sync Multiplexer

1:2 Multiplexer Mode

The MAX4885 provides two modes of operation for the HSYNC and VSYNC signals. In 1:2 mode (M = 0), the HSYNC/VSYNC inputs are buffered to provide level shifting and drive capability to meet the VESA specification.

2:1 Multiplexer Mode

In 2:1 mode (M = 1), the HSYNC/VSYNC output buffers are disabled, and switches pass signals directly. The HSYNC and VSYNC switches/buffers are identical, and either input can be used to route HSYNC and VSYNC signals.

Display Data Channel Multiplexer

The MAX4885 provides two voltage-clamped switches to route DDC signals (see Table 3). Each switch clamps signals to a diode drop less than the voltage applied on V_{CL}. Supply +3.3V on V_{CL} to provide voltage clamping for VESA I^2C-compatible signals. If voltage clamping is not required, connect V_{CL} to V+. The DDCA and DDCB switches are identical, and each switch can be used to route either DDC signal.

ESD Protection

As with all Maxim devices, ESD-protection structures are incorporated on all pins to protect against electrostatic discharges encountered during handling and assembly. Additionally, the MAX4885 is protected to ±8kV on RGB, HSYNC, VSYNC, and DDC switches by the Human Body Model (HBM). For optimum ESD performance, bypass each V+ pin to ground with a 0.1µF or larger ceramic capacitor.

Human Body Model (HBM)

Several ESD testing standards exist for measuring the robustness of ESD structures. The ESD protection of the MAX4885 is characterized with the Human Body Model. Figure 5 shows the model used to simulate an ESD event resulting from contact with the human body. The model consists of a 100pF storage capacitor that is charged to a high voltage, then discharged through a 1.5kΩ resistor. Figure 6 shows the current waveform when the storage capacitor is discharged into a low impedance.

ESD Test Conditions

ESD performance depends on a variety of conditions. Please contact Maxim for a reliability report documenting test setup, methodology, and results.

Table 2. HV Truth Table

$\overline{EN}$	M	SEL	FUNCTION
0	0	0	1:2 Mode Buffers Enabled H0 to H1 V0 to V1
0	0	1	1:2 Mode Buffers Enabled H0 to H2 V0 to V2
0	1	0	2:1 Mode Buffers Disabled H0 to H1 V0 to V1
0	1	1	2:1 Mode Buffers Disabled H0 to H2 V0 to V2
1	X	X	H_, V_ High Impedance

X = Don't Care

Table 3. DDC Truth Table

$\overline{EN}$	SEL	FUNCTION
0	0	DDCA0 to DDCA1 DDCB0 to DDCB1
0	1	DDCA0 to DDCA2 DDCB0 to DDCB2
1	X	DDCA_, DDCB_ High Impedance

X = Don't Care

Applications Information

1:2 Multiplexer for Low-Voltage Graphics Controllers

The MAX4885 provides the level shifting necessary to drive two standard VGA ports from a graphics controller as low as +2.2V. In 1:2 mode, internal buffers drive the HSYNC and VSYNC signals to VGA standard TTL levels. The DDC multiplexer provides level shifting by clamping signals to a diode drop less than V_{CL} (see the *Typical Operating Circuit*). Connect V_{CL} to +3.3V for normal operation, or to V+ to disable voltage clamping for DDC signals.

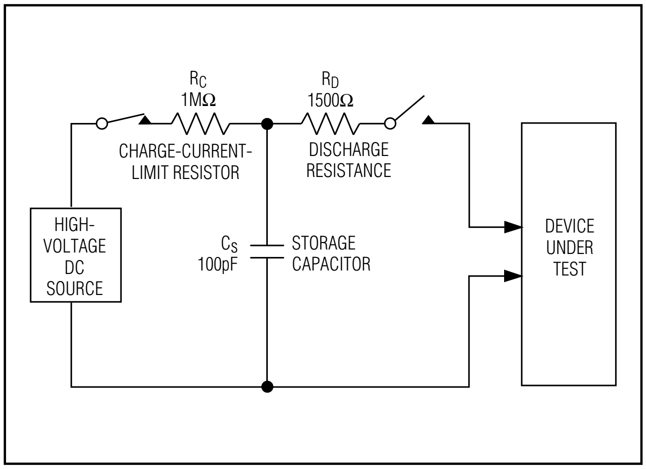


Figure 5. Human Body ESD Test Model

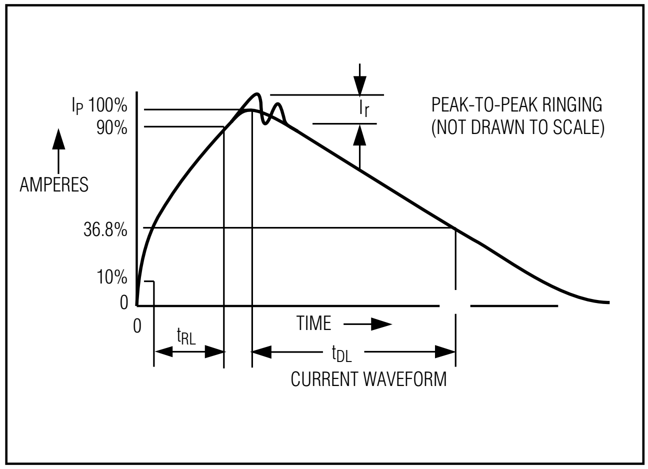


Figure 6. HBM Discharge Current Waveform

2:1 Multiplexer

In 2:1 mode, HSYNC and VSYNC buffers are disabled, allowing bidirectional signaling. The DDC multiplexer provides level shifting by clamping signals to a diode drop less than V_{CL} (see the *Typical Operating Circuit*). Connect V_{CL} to V+ to disable voltage clamping for DDC signals.

Power-Supply Decoupling

Bypass each V+ pin and V_{CL} to ground with a 0.1µF or larger ceramic capacitor as close to the device as possible.

PC Board Layout

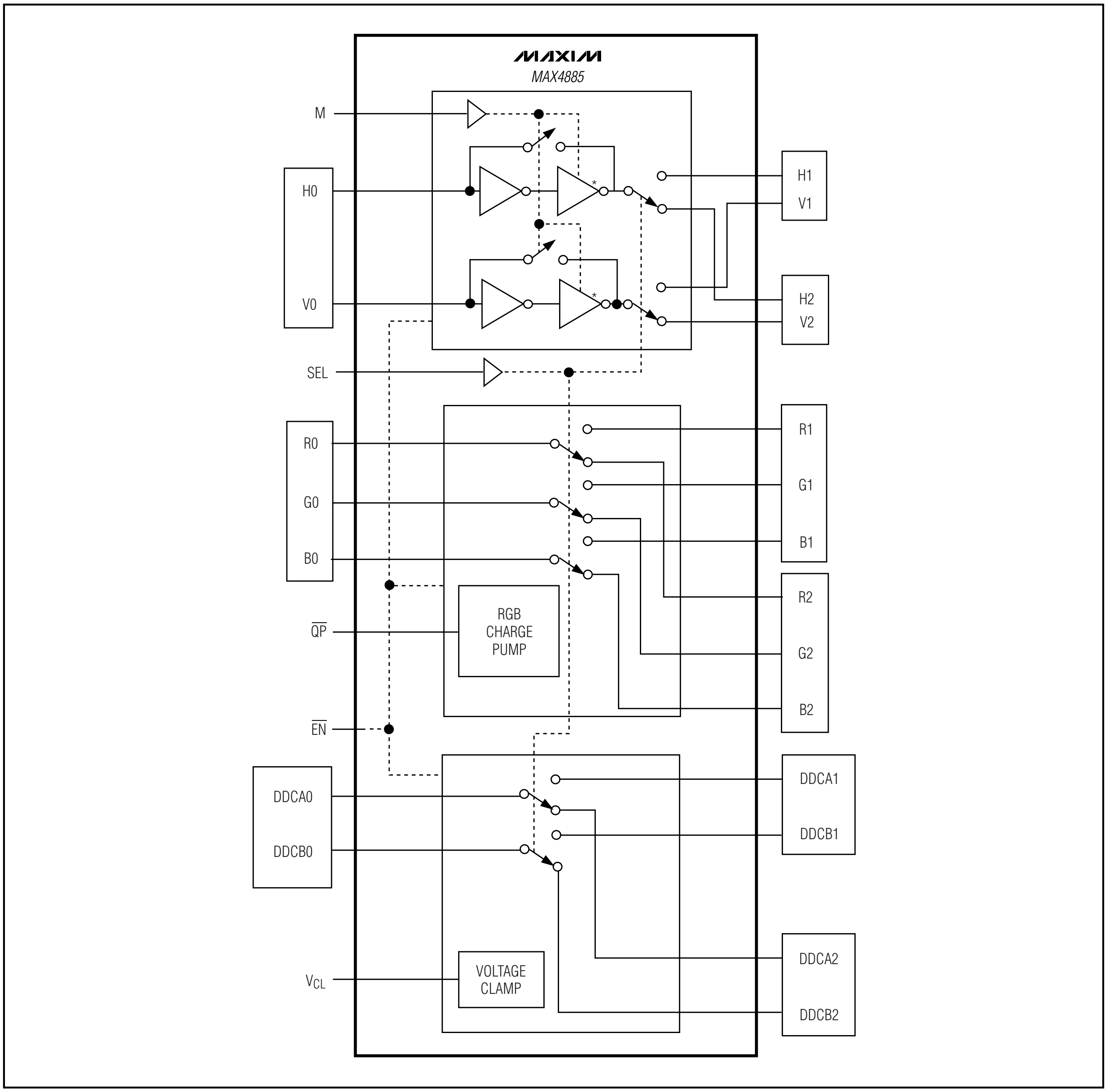
High-speed switches such as the MAX4885 require proper PC board layout for optimum performance. Ensure that impedance-controlled PC board traces for high-speed signals are matched in length and as short as possible. Connect the exposed pad to a solid ground plane.

Chip Information

PROCESS: BiCMOS

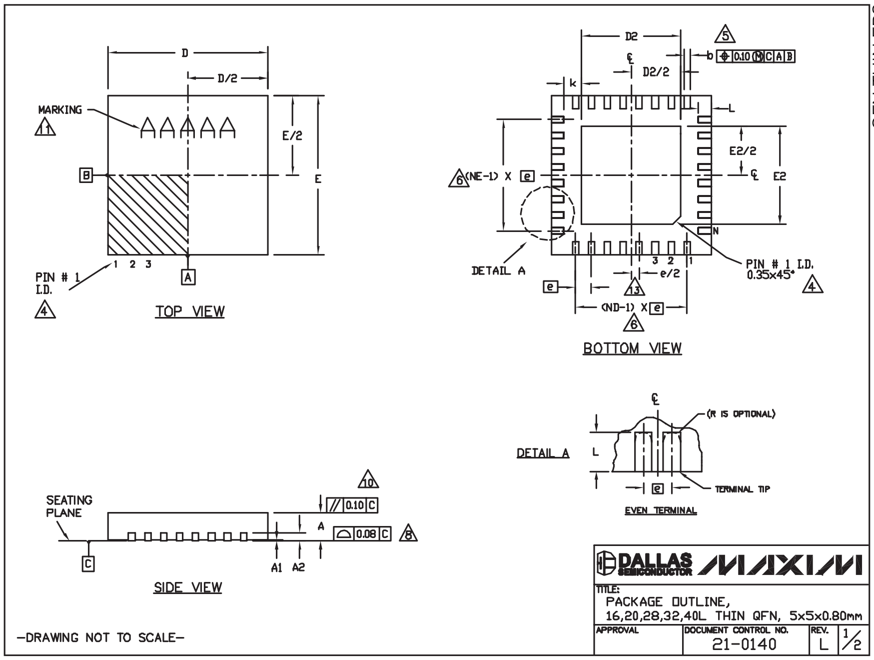
CONNECT EXPOSED PAD TO GND

Functional Diagram



Package Information

(The package drawing(s) in this data sheet may not reflect the most current specifications. For the latest package outline information, go to **www.maxim-ic.com/packages**.)



QFN THIN.EPS

COMMON DIMENSIONS															
PKG.	16L 5x5			20L 5x5			28L 5x5			32L 5x5			40L 5x5		
SYMBOL	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
A	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80	0.70	0.75	0.80
A1	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05	0	0.02	0.05
A2	0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.			0.20 REF.		
b	0.25	0.30	0.35	0.25	0.30	0.35	0.20	0.25	0.30	0.20	0.25	0.30	0.15	0.20	0.25
D	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
E	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10	4.90	5.00	5.10
e	0.80 BSC.			0.65 BSC.			0.50 BSC.			0.50 BSC.			0.40 BSC.		
k	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-	0.25	-	-
L	0.30	0.40	0.50	0.45	0.55	0.65	0.45	0.55	0.65	0.30	0.40	0.50	0.30	0.40	0.50
N	16			20			28			32			40		
ND	4			5			7			8			10		
NE	4			5			7			8			10		
JEDEC	WHHB			WHHC			WHHD-1			WHHD-2			-----		

EXPOSED PAD VARIATIONS						
PKG. CODES	D2			E2		
	MIN.	NOM.	MAX.	MIN.	NOM.	MAX.
T1655-2	3.00	3.10	3.20	3.00	3.10	3.20
T1655-3	3.00	3.10	3.20	3.00	3.10	3.20
T1655N-1	3.00	3.10	3.20	3.00	3.10	3.20
T2055-3	3.00	3.10	3.20	3.00	3.10	3.20
T2055-4	3.00	3.10	3.20	3.00	3.10	3.20
T2055-5	3.15	3.25	3.35	3.15	3.25	3.35
T2055MN-5	3.15	3.25	3.35	3.15	3.25	3.35
T2855-3	3.15	3.25	3.35	3.15	3.25	3.35
T2855-4	2.60	2.70	2.80	2.60	2.70	2.80
T2855-5	2.60	2.70	2.80	2.60	2.70	2.80
T2855-6	3.15	3.25	3.35	3.15	3.25	3.35
T2855-7	2.60	2.70	2.80	2.60	2.70	2.80
T2855-8	3.15	3.25	3.35	3.15	3.25	3.35
T2855N-1	3.15	3.25	3.35	3.15	3.25	3.35
T3255-3	3.00	3.10	3.20	3.00	3.10	3.20
T3255-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255M-4	3.00	3.10	3.20	3.00	3.10	3.20
T3255-5	3.00	3.10	3.20	3.00	3.10	3.20
T3255N-1	3.00	3.10	3.20	3.00	3.10	3.20
T4055-1	3.40	3.50	3.60	3.40	3.50	3.60
T4055-2	3.40	3.50	3.60	3.40	3.50	3.60
T4055MN-1	3.40	3.50	3.60	3.40	3.50	3.60

NOTES:

1. DIMENSIONING & TOLERANCING CONFORM TO ASME Y14.5M-1994.
2. ALL DIMENSIONS ARE IN MILLIMETERS. ANGLES ARE IN DEGREES.
3. N IS THE TOTAL NUMBER OF TERMINALS.
4. THE TERMINAL #1 IDENTIFIER AND TERMINAL NUMBERING CONVENTION SHALL CONFORM TO JESD 95-1 SPP-012. DETAILS OF TERMINAL #1 IDENTIFIER ARE OPTIONAL, BUT MUST BE LOCATED WITHIN THE ZONE INDICATED. THE TERMINAL #1 IDENTIFIER MAY BE EITHER A MOLD OR MARKED FEATURE.
5. DIMENSION b APPLIES TO METALLIZED TERMINAL AND IS MEASURED BETWEEN 0.25 mm AND 0.30 mm FROM TERMINAL TIP.
6. ND AND NE REFER TO THE NUMBER OF TERMINALS ON EACH D AND E SIDE RESPECTIVELY.
7. DEPOPULATION IS POSSIBLE IN A SYMMETRICAL FASHION.
8. COPLANARITY APPLIES TO THE EXPOSED HEAT SINK SLUG AS WELL AS THE TERMINALS.
9. DRAWING CONFORMS TO JEDEC MO220, EXCEPT EXPOSED PAD DIMENSION FOR T2855-3, T2855-6, T4055-1 AND T4055-2.
10. WARPAGE SHALL NOT EXCEED 0.10 mm.
11. MARKING IS FOR PACKAGE ORIENTATION REFERENCE ONLY.
12. NUMBER OF LEADS SHOWN ARE FOR REFERENCE ONLY.
13. LEAD CENTERLINES TO BE AT TRUE POSITION AS DEFINED BY BASIC DIMENSION 'e', ±0.05.
14. ALL DIMENSIONS APPLY TO BOTH LEADED AND PbFREE PARTS.

-DRAWING NOT TO SCALE-

DALLAS SEMICONDUCTOR MAXIM

TITLE: PACKAGE OUTLINE, 16,20,28,32,40L THIN QFN, 5x5x0.80mm

APPROVAL	DOCUMENT CONTROL NO.	REV.	
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